University of California at Berkeley
Physics 111 Laboratory
Basic Semiconductor Circuits (BSC)

Lab 11

Digital Circuits 555 Timer

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Reading:

Horowitz & Hill	Chapter 5.14
Hayes & Horowitz	Pages 214-215
Millman & Grabel	Pages 690-692
Senturia & Wedlock	Pages 526-535

In this lab you will learn about the the 555 timer chip and its varied applications.

Pre-lab questions:

1. Explain the monostable and astable modes of the 555 timer qualitatively.

2. Derive the equations for the oscillator circuit based on the explanation given in Section 11.1 and in the specifications. Find the frequency and duty cycle of the circuit as functions of R_A, R_B, and C.

3. Derive the equation for pulse duration in terms of R and C for the 555 in monostable mode (see Section 11.2).

In the lab:

The 555 timer circuit

The NE555 timer chip is a chip with a tremendous range of applications in digital circuits and analog-digital interfaces.

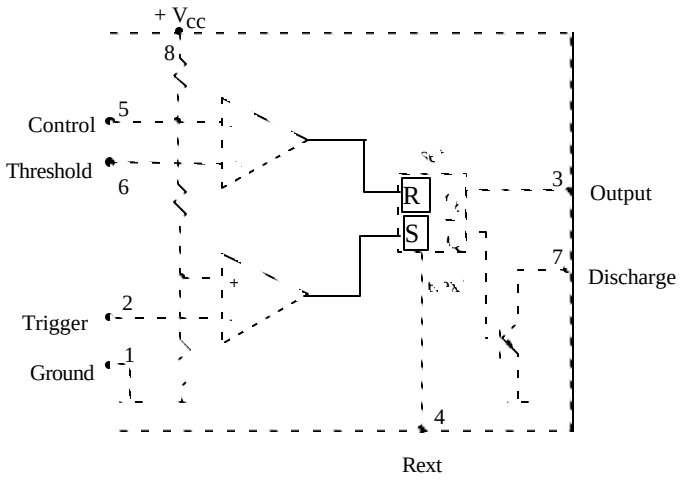


Figure 11.1 Schematic diagram of the NE555 timer chip

11.1 The 555 can be used as an oscillator ("astable" mode) in the circuit shown in Figure 11.2:

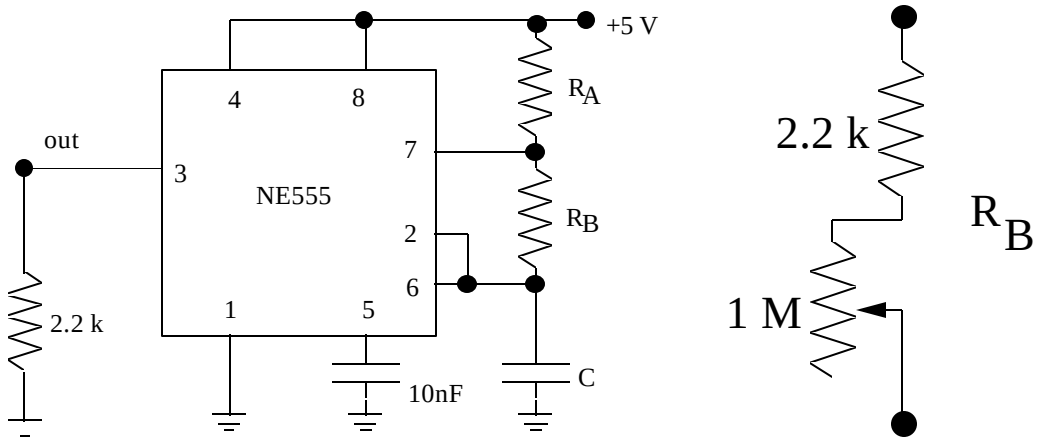


Figure 11.2 NE555 oscillator circuit

The circuit works as follows: initially, the flip-flop ('flop') in the 555 is set, and the discharge transistor does not conduct. C charges up via R_A and R_B until the voltage across the capacitor C reaches 2/3 of V_{cc}. At this point, the upper comparator switches and the flip-flop is reset to low (L). The discharge transistor starts conducting and discharges C via R_B, until the voltage at C falls below 1/3 of V_{cc}, at which point the lower comparator (pin 2) switches and sets the flop again. Also see the specification sheets.

Build the circuit in Figure 11.2 using 2.2 kΩ for R_A, another 2.2 kΩ in series with a 1 MegΩ potentiometer for R_B (as shown in Figure 11.2), and 360 pF for C. Determine the frequency range that can be achieved by varying the potentiometer, and compare with the theoretical range based on the equations given in the NE555 data sheets (see Appendix). Measure the frequency and duty cycle (fraction of time the output spends in the high state) for several potentiometer settings, and compare to predicted values (see Pre-lab Question 2). **Note:** the data sheets use a slightly different and unusual definition of the duty cycle.

11.2 Now build the circuit in Figure 11.3 using the 555 as a single-pulse generator ("monostable" mode):

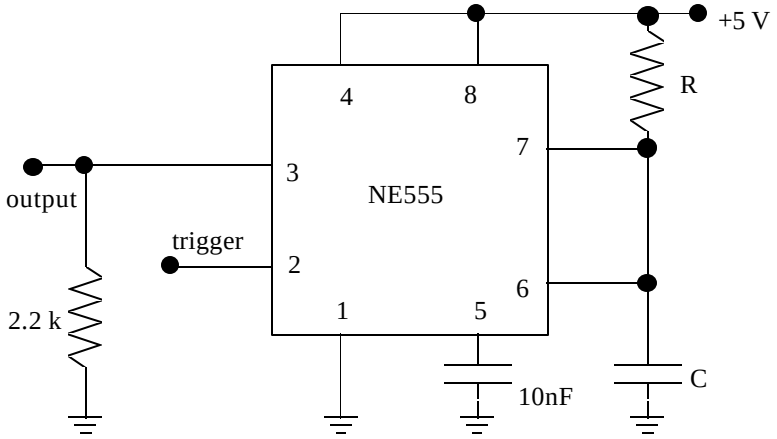


Figure 11.3 Using NE555 in the single-pulse monostable mode

Pick R and C such that the pulse duration is 1 second (see data sheets), and verify the proper operation of the circuit. **Note:** it is very important that the capacitor C must **not** be an electrolytic capacitor; choose its value accordingly! Explain how the circuit works, clearly indicating the manner in which you trigger it.

The 555 can also be used to generate frequency-modulated signals or pulse-width modulated signals (see data sheets). Feel free to experiment!

Some applications

11.3 Design and build a digital frequency meter. The input signal is a 0 to 5V square wave from the function generator and is connected to the 7490s via a gate; the gate is opened for exactly one

second using the 555 in its monostable mode. One push button is used to start the 555; one second later the frequency is displayed. Another push button resets the display. (This circuit can also be designed with one switch to do both functions.) The 7490s are read out via the 7-segment displays. Test your frequency meter by setting the function generator to frequencies between a few Hz and 100 Hz.

11.4 Modify the previous circuit, with some simple changes, into a two-digit digital stopwatch. It's supposed to work like the real thing: there are two push buttons; pushing the first button once starts it, pushing it a second time stops it. The other push button resets it. Remember that the push buttons bounce. However, since they have only one contact instead of alternating between two, the "classical" debouncing scheme using a flip-flop cannot be applied. **Hint:** one solution uses a 555 in its monostable mode. Use the function generator to generate a 1 Hz or 0.1 Hz clock. You may need one additional 7490.

Questions:

There are no questions for this week's lab.

Appendix Data sheet for NE555 next page.

May 1997

National Semiconductor

LM555/LM555C Timer

General Description

The LM555 is a highly stable device for generating accurate time delays or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and duty cycle are accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output circuit can source or sink up to 200 mA or drive TTL circuits.

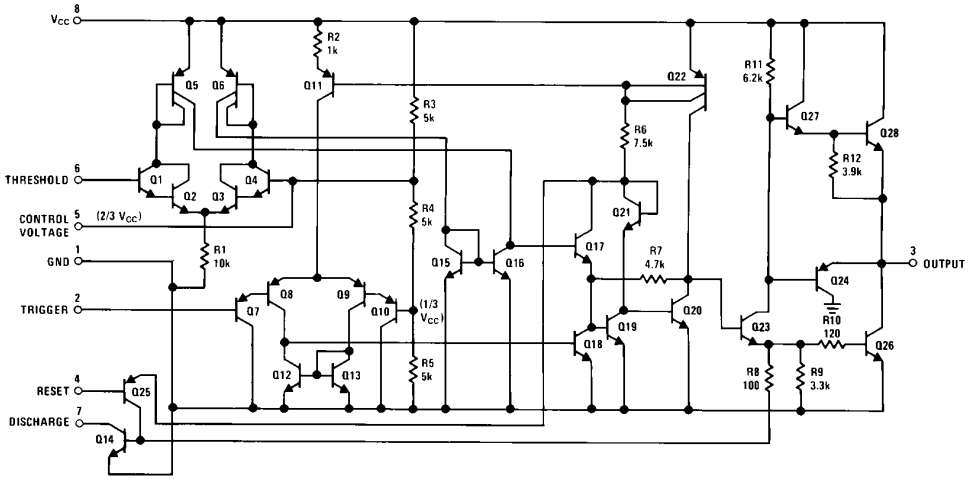
Features

- Direct replacement for SE555/NE555
- Timing from microseconds through hours
- Operates in both astable and monostable modes
- Adjustable duty cycle
- Output can source or sink 200 mA
- Output and supply TTL compatible
- Temperature stability better than 0.005% per ˚C
- Normally on and normally off output
- Available in 8 pin MSOP package

Applications

- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Linear ramp generator

Schematic Diagram



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Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	+18V
Power Dissipation (Note 3)	
LM555H, LM555CH	760 mW
LM555, LM555CN	1180 mW
LM555CMM	613 mW
Operating Temperature Ranges	
LM555C	0˚C to +70˚C
LM555	−55˚C to + 125˚C
Storage Temperature Range	−65˚C to +150˚C
Soldering Information	
Dual-In-Line Package	
Soldering (10 Seconds)	260˚C
Small Outline Packages	
(SOIC and MSOP)	
Vapor Phase (60 Seconds)	215˚C
Infrared (15 Seconds)	220˚C

See AN-450 “Surface Mounting Methods and Their Effect on Product Reliability” for other methods of soldering surface mount devices.

Electrical Characteristics (Notes 1, 2)

(T_A = 25˚C, V_{CC} = +5V to +15V, unless othewise specified)

Parameter	Conditions	Limits						Units
		LM555			LM555C			
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage		4.5		18	4.5		16	V
Supply Current	V_{CC} = 5V, R_L = ∞		3	5		3	6	mA
	V_{CC} = 15V, R_L = ∞		10	12		10	15	mA
	(Low State) (Note 4)							
Timing Error, Monostable								
Initial Accuracy			0.5			1		%
Drift with Temperature	R_A = 1k to 100 kΩ,		30			50		ppm/˚C
	C = 0.1 µF, (Note 5)							
Accuracy over Temperature			1.5			1.5		%
Drift with Supply			0.05			0.1		%/V
Timing Error, Astable								
Initial Accuracy			1.5			2.25		%
Drift with Temperature	R_A, R_B = 1k to 100 kΩ,		90			150		ppm/˚C
	C = 0.1 µF, (Note 5)							
Accuracy over Temperature			2.5			3.0		%
Drift with Supply			0.15			0.30		%/V
Threshold Voltage			0.667			0.667		x V_{CC}
Trigger Voltage	V_{CC} = 15V	4.8	5	5.2		5		V
	V_{CC} = 5V	1.45	1.67	1.9		1.67		V
Trigger Current			0.01	0.5		0.5	0.9	µA
Reset Voltage		0.4	0.5	1	0.4	0.5	1	V
Reset Current			0.1	0.4		0.1	0.4	mA
Threshold Current	(Note 6)		0.1	0.25		0.1	0.25	µA
Control Voltage Level	V_{CC} = 15V	9.6	10	10.4	9	10	11	V
	V_{CC} = 5V	2.9	3.33	3.8	2.6	3.33	4	V
Pin 7 Leakage Output High			1	100		1	100	nA
Pin 7 Sat (Note 7)								
Output Low	V_{CC} = 15V, I_7 = 15 mA		150			180		mV
Output Low	V_{CC} = 4.5V, I_7 = 4.5 mA		70	100		80	200	mV

Electrical Characteristics (Notes 1, 2) (Continued)

(T_A = 25˚C, V_{CC} = +5V to +15V, unless othewise specified)

Parameter	Conditions	Limits						Units
		LM555			LM555C			
		Min	Typ	Max	Min	Typ	Max	
Output Voltage Drop (Low)	V_{CC} = 15V							
	I_{SINK} = 10 mA		0.1	0.15		0.1	0.25	V
	I_{SINK} = 50 mA		0.4	0.5		0.4	0.75	V
	I_{SINK} = 100 mA		2	2.2		2	2.5	V
	I_{SINK} = 200 mA		2.5			2.5		V
	V_{CC} = 5V							
	I_{SINK} = 8 mA		0.1	0.25				V
	I_{SINK} = 5 mA					0.25	0.35	V
Output Voltage Drop (High)	I_{SOURCE} = 200 mA, V_{CC} = 15V		12.5			12.5		V
	I_{SOURCE} = 100 mA, V_{CC} = 15V	13	13.3		12.75	13.3		V
	V_{CC} = 5V	3	3.3		2.75	3.3		V
Rise Time of Output			100			100		ns
Fall Time of Output			100			100		ns

Note 1: All voltages are measured with respect to the ground pin, unless otherwise specified.

Note 2: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 3: For operating at elevated temperatures the device must be derated above 25˚C based on a +150˚C maximum junction temperature and a thermal resistance of 164˚C/W (T0-5), 106˚C/W (DIP), 170˚C/W (S0-8), and 204˚C/W (MSOP) junction to ambient.

Note 4: Supply current when output high typically 1 mA less at V_{CC} = 5V.

Note 5: Tested at V_{CC} = 5V and V_{CC} = 15V.

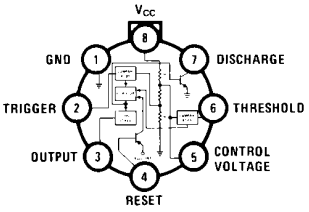
Note 6: This will determine the maximum value of $R_A + R_B$ for 15V operation. The maximum total ($R_A + R_B$) is 20 MΩ.

Note 7: No protection against excessive pin 7 current is necessary providing the package dissipation rating will not be exceeded.

Note 8: Refer to RETS555X drawing of military LM555H and LM555J versions for specifications.

Connection Diagrams

Metal Can Package



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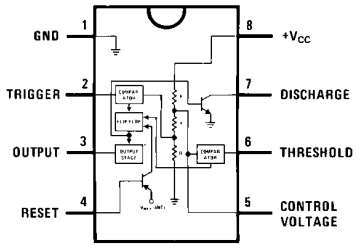
Top View
Order Number LM555H or LM555CH
See NS Package Number H08C

Dual-In-Line, Small Outline and Molded Mini Small Outline Packages



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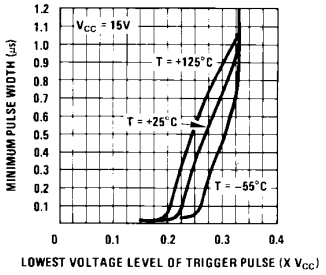
Top View
Order Number LM555J, LM555CJ, LM555CM, LM555CMM or LM555CN
See NS Package Number J08A, M08A, MUA08A or N08E

Typical Performance Characteristics

Minimuim Pulse Width Required for Triggering



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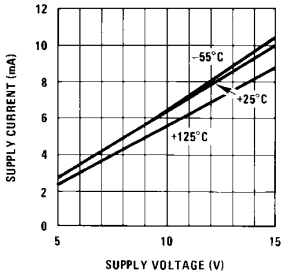
Supply Current vs Supply Voltage



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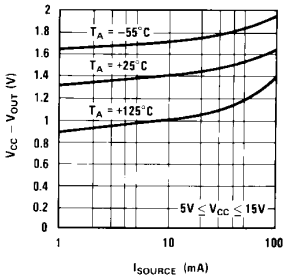
High Output Voltage vs Output Source Current



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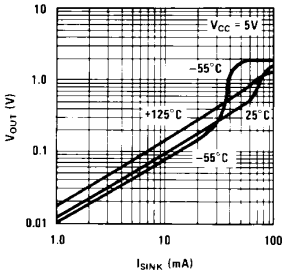
Low Output Voltage vs Output Sink Current



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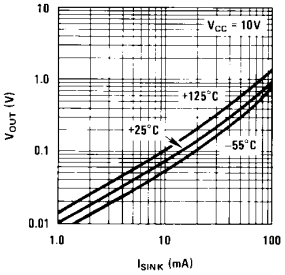
Low Output Voltage vs Output Sink Current



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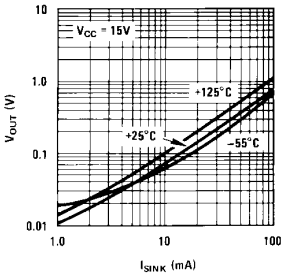
Low Output Voltage vs Output Sink Current



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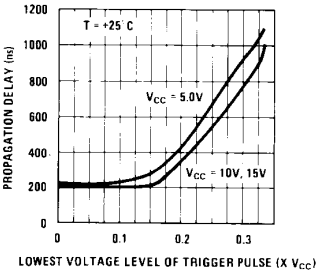
Output Propagation Delay vs Voltage Level of Trigger Pulse



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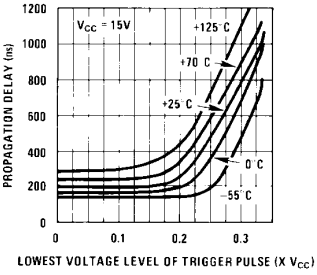
Output Propagation Delay vs Voltage Level of Trigger Pulse



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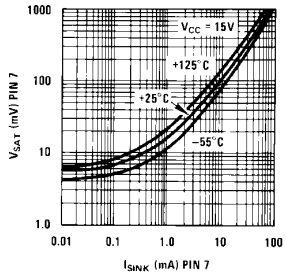
Discharge Transistor (Pin 7) Voltage vs Sink Current



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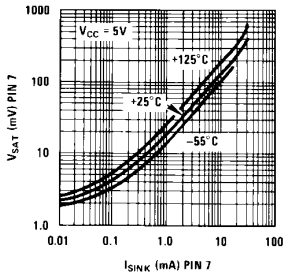
Typical Performance Characteristics (Continued)

Discharge Transistor (Pin 7) Voltage vs Sink Current



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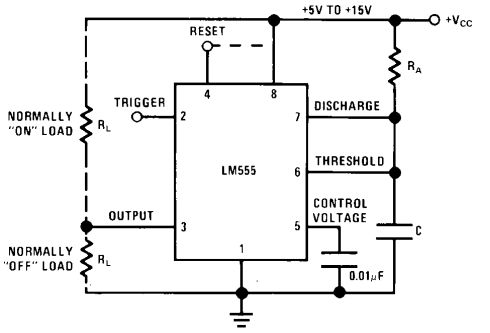
Applications Information

MONOSTABLE OPERATION

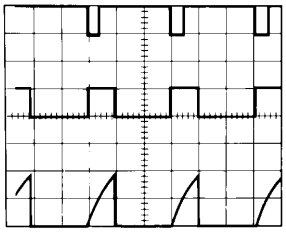
In this mode of operation, the timer functions as a one-shot (*Figure 1*). The external capacitor is initially held discharged by a transistor inside the timer. Upon application of a negative trigger pulse of less than 1/3 V_{CC} to pin 2, the flip-flop is set which both releases the short circuit across the capacitor and drives the output high.



DS007851-5

FIGURE 1. Monostable

The voltage across the capacitor then increases exponentially for a period of t = 1.1 R_A C, at the end of which time the voltage equals 2/3 V_{CC}. The comparator then resets the flip-flop which in turn discharges the capacitor and drives the output to its low state. *Figure 2* shows the waveforms generated in this mode of operation. Since the charge and the threshold level of the comparator are both directly proportional to supply voltage, the timing internal is independent of supply.



DS007851-6

V_{CC} = 5V Top Trace: Input 5V/Div.
TIME = 0.1 ms/DIV. Middle Trace: Output 5V/Div.
R_A = 9.1 kΩ Bottom Trace: Capacitor Voltage 2V/Div.
C = 0.01 μF

FIGURE 2. Monostable Waveforms

During the timing cycle when the output is high, the further application of a trigger pulse will not effect the circuit so long as the trigger input is returned high at least 10 μs before the end of the timing interval. However the circuit can be reset during this time by the application of a negative pulse to the reset terminal (pin 4). The output will then remain in the low state until a trigger pulse is again applied.

When the reset function is not in use, it is recommended that it be connected to V_{CC} to avoid any possibility of false triggering.

Figure 3 is a nomograph for easy determination of R, C values for various time delays.

NOTE: In monostable operation, the trigger should be driven high before the end of timing cycle.

Applications Information (Continued)

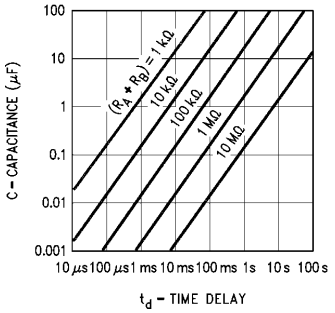


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FIGURE 3. Time Delay

ASTABLE OPERATION

If the circuit is connected as shown in *Figure 4* (pins 2 and 6 connected) it will trigger itself and free run as a multivibrator. The external capacitor charges through $R_A + R_B$ and discharges through R_B. Thus the duty cycle may be precisely set by the ratio of these two resistors.

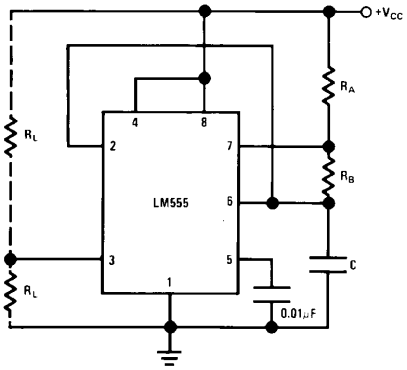

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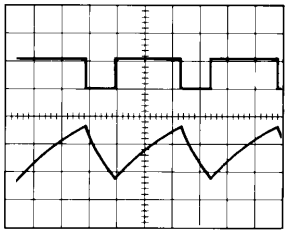
FIGURE 4. Astable

In this mode of operation, the capacitor charges and discharges between 1/3 V_{CC} and 2/3 V_{CC}. As in the triggered mode, the charge and discharge times, and therefore the frequency are independent of the supply voltage.

Figure 5 shows the waveforms generated in this mode of operation.



DS007851-9

V_{CC} = 5V
TIME = 20 μs/DIV.
R_A = 3.9 kΩ
R_B = 3 kΩ
C = 0.01 μF

Top Trace: Output 5V/Div.
Bottom Trace: Capacitor Voltage 1V/Div.

FIGURE 5. Astable Waveforms

The charge time (output high) is given by:

$$t_1 = 0.693\ (R_A + R_B)\ C$$

And the discharge time (output low) by:

$$t_2 = 0.693\ (R_B)\ C$$

Thus the total period is:

$$T = t_1 + t_2 = 0.693\ (R_A + 2R_B)\ C$$

The frequency of oscillation is:

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B)\ C}$$

Figure 6 may be used for quick determination of these RC values.

The duty cycle is:

$$D = \frac{R_B}{R_A + 2R_B}$$

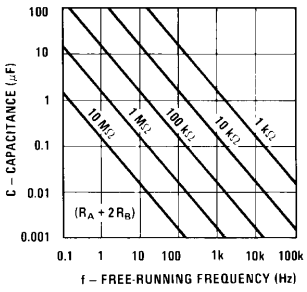


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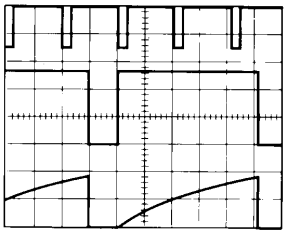
FIGURE 6. Free Running Frequency

FREQUENCY DIVIDER

The monostable circuit of *Figure 1* can be used as a frequency divider by adjusting the length of the timing cycle. *Figure 7* shows the waveforms generated in a divide by three circuit.

Applications Information (Continued)



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V_{CC} = 5V Top Trace: Input 4V/Div.
TIME = 20 µs/DIV. Middle Trace: Output 2V/Div.
R_A = 9.1 kΩ Bottom Trace: Capacitor 2V/Div.
C = 0.01 µF

FIGURE 7. Frequency Divider

PULSE WIDTH MODULATOR

When the timer is connected in the monostable mode and triggered with a continuous pulse train, the output pulse width can be modulated by a signal applied to pin 5. *Figure 8* shows the circuit, and in *Figure 9* are some waveform examples.

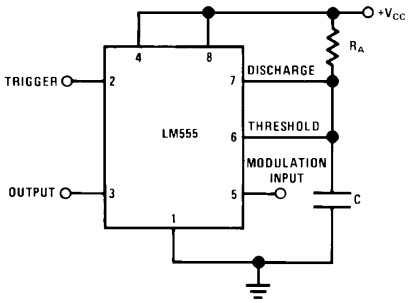

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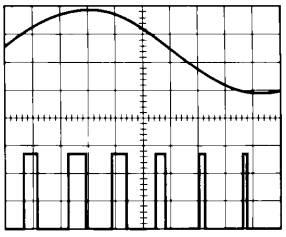
FIGURE 8. Pulse Width Modulator



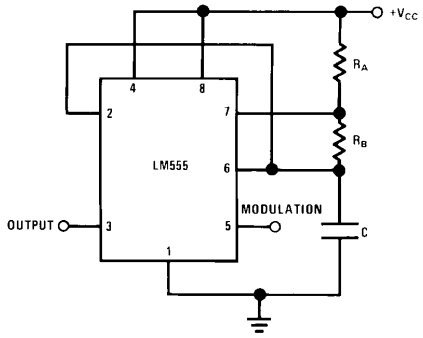
DS007851-13

V_{CC} = 5V Top Trace: Modulation 1V/Div.
TIME = 0.2 ms/DIV. Bottom Trace: Output Voltage 2V/Div.
R_A = 9.1 kΩ
C = 0.01 µF

FIGURE 9. Pulse Width Modulator

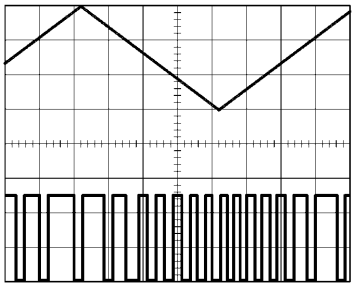
PULSE POSITION MODULATOR

This application uses the timer connected for astable operation, as in *Figure 10*, with a modulating signal again applied to the control voltage terminal. The pulse position varies with the modulating signal, since the threshold voltage and hence the time delay is varied. *Figure 11* shows the waveforms generated for a triangle wave modulation signal.



DS007851-14

FIGURE 10. Pulse Position Modulator



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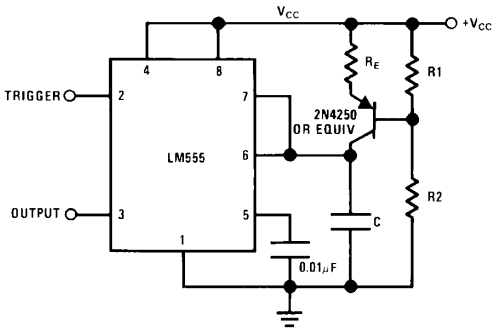
V_{CC} = 5V Top Trace: Modulation Input 1V/Div.
TIME = 0.1 ms/DIV. Bottom Trace: Output 2V/Div.
R_A = 3.9 kΩ
R_B = 3 kΩ
C = 0.01 µF

FIGURE 11. Pulse Position Modulator

LINEAR RAMP

When the pullup resistor, R_A, in the monostable circuit is replaced by a constant current source, a linear ramp is generated. *Figure 12* shows a circuit configuration that will perform this function.



DS007851-16

FIGURE 12.

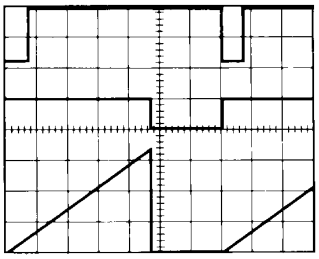
Applications Information (Continued)

Figure 13 shows waveforms generated by the linear ramp. The time interval is given by:

$$T = \frac{2/3\ V_{CC}\ R_E\ (R_1 + R_2)\ C}{R_1\ V_{CC} - V_{BE}\ (R_1 + R_2)}$$

$$V_{BE} \cong 0.6V$$

$$V_{BE} \cong 0.6V$$



DS007851-17

V_{CC} = 5V
TIME = 20 µs/DIV.
R_1 = 47 kΩ
R_2 = 100 kΩ
R_E = 2.7 kΩ
C = 0.01 µF

Top Trace: Input 3V/Div.
Middle Trace: Output 5V/Div.
Bottom Trace: Capacitor Voltage 1V/Div.

FIGURE 13. Linear Ramp

50% DUTY CYCLE OSCILLATOR

For a 50% duty cycle, the resistors R_A and R_B may be connected as in *Figure 14*. The time period for the output high is the same as previous, $t_1 = 0.693\ R_A\ C$. For the output low it is t_2 =

$$\left[(R_A\ R_B)/(R_A + R_B)\right]\ C\ \ell n\left[\frac{R_B - 2R_A}{2R_B - R_A}\right]$$

Thus the frequency of oscillation is

$$f = \frac{1}{t_1 + t_2}$$

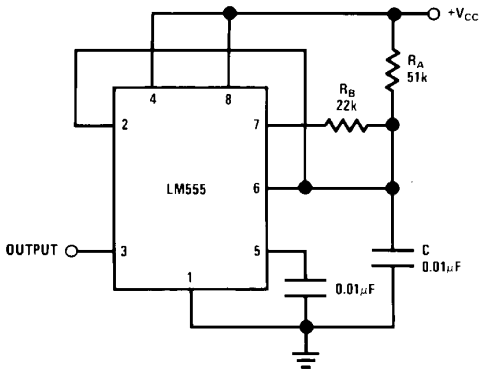


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FIGURE 14. 50% Duty Cycle Oscillator

Note that this circuit will not oscillate if R_B is greater than 1/2 R_A because the junction of R_A and R_B cannot bring pin 2 down to 1/3 V_{CC} and trigger the lower comparator.

ADDITIONAL INFORMATION

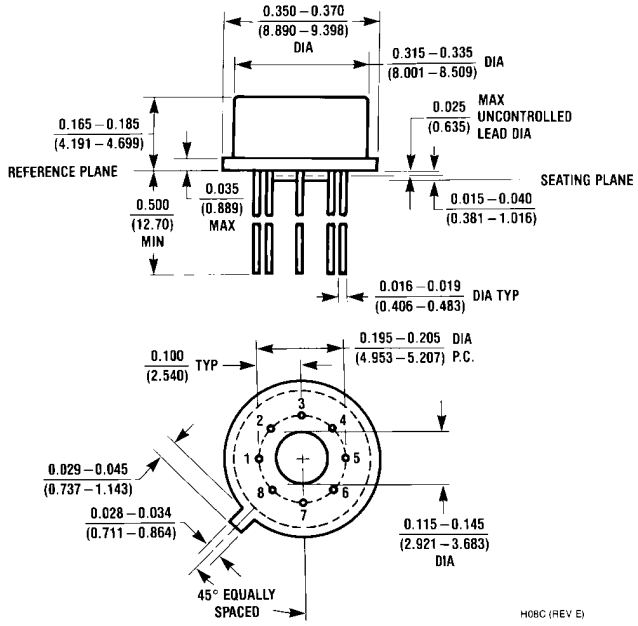
Adequate power supply bypassing is necessary to protect associated circuitry. Minimum recommended is 0.1 µF in parallel with 1 µF electrolytic.

Lower comparator storage time can be as long as 10 µs when pin 2 is driven fully to ground for triggering. This limits the monostable pulse width to 10 µs minimum.

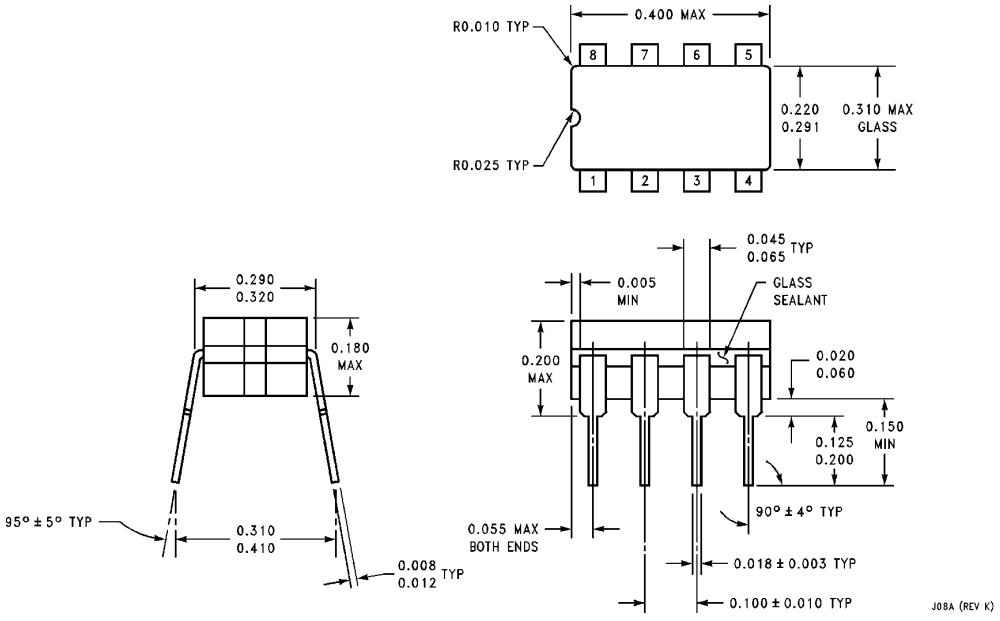
Delay time reset to output is 0.47 µs typical. Minimum reset pulse width must be 0.3 µs, typical.

Pin 7 current switches within 30 ns of the output (pin 3) voltage.

Physical Dimensions inches (millimeters)

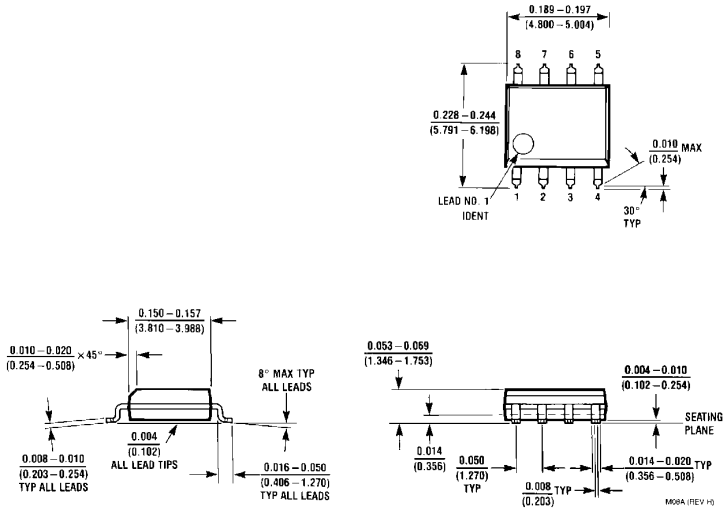


Metal Can Package (H)
Order Number LM555H or LM555CH
NS Package Number H08C



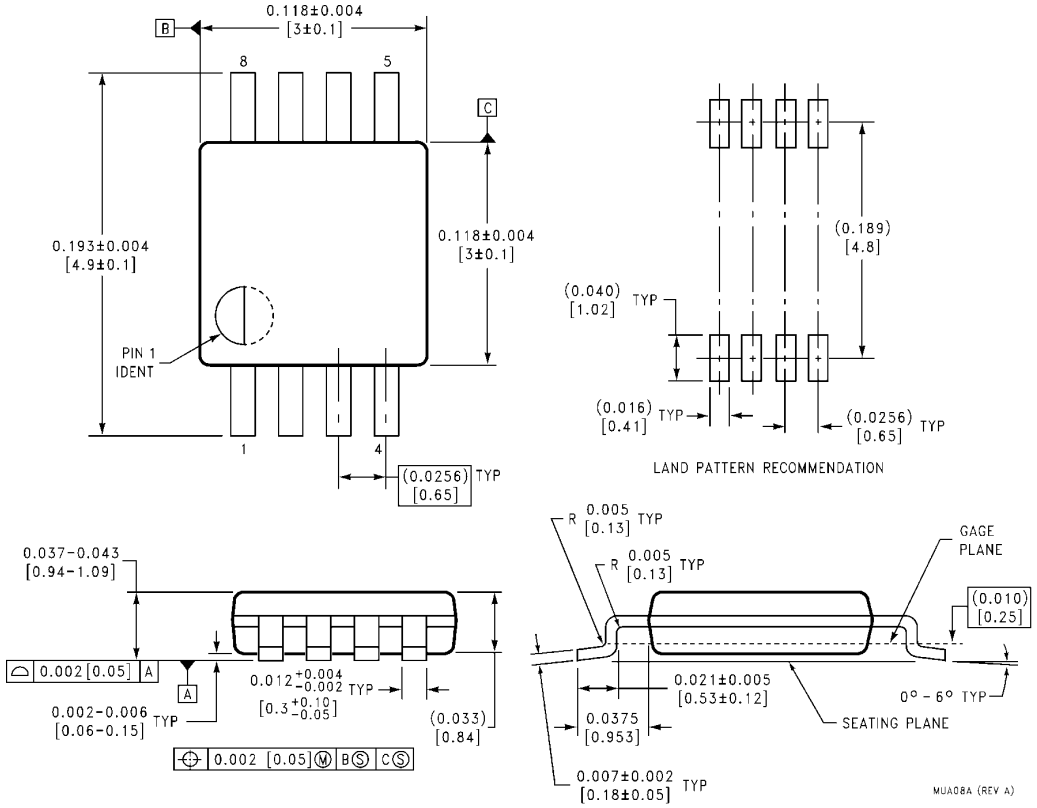
Ceramic Dual-In-Line Package (J)
Order Number LM555J or LM555CJ
NS Package Number J08A

Physical Dimensions inches (millimeters) (Continued)



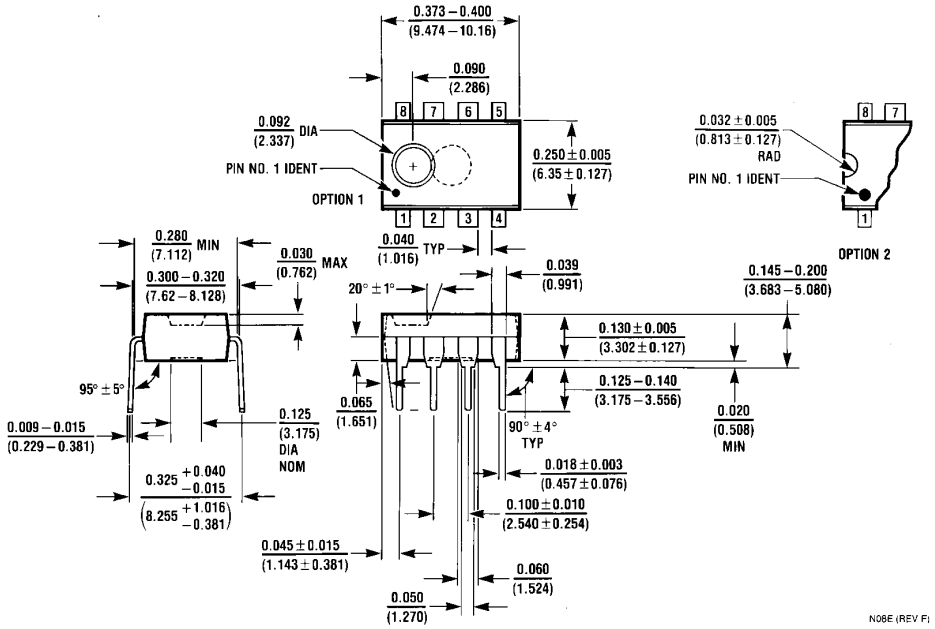
Small Outline Package (M)
Order Number LM555CM
NS Package Number M08A

Physical Dimensions inches (millimeters) (Continued)



8-Lead (0.118" Wide) Molded Mini Small Outline Package
Order Number LM555CMM
NS Package Number MUA08A

Physical Dimensions inches (millimeters) (Continued)



Molded Dual-In-Line Package (N)
Order Number LM555CN
NS Package Number N08E

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